DRIFT STEP RECOVERY DIODE TRANSMITTER FOR HIGH POWER GPR DESIGN

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ABSTRACT

Some elements of the modern ground penetrating radar (GPR) determine its performance factor, resolution and depth of sounding. There are impulse transmitter, ultra-wide-band receiver as well as transmitting and receiver antennas. Improvement of the GPR's parameters is usually achieved by modernization of receiving circuits, antenna design, decreasing of input noises and using of complex computational algorithms for on-line and post-processing. As active element for impulse generation are widely used step recovery diodes (SRDs) or avalanche transistors. However such devices can not generate nanosecond pulses up to some hundreds volts on the antenna terminal.

This work is devoted to application of drift step recovery diodes (DSRDs) in GPR transmitter design. Current drive circuit based on charge DSRD model has been computed and optimized. Investigation results for pulse generator characterized by peak power up to 5 kW and rise times as small as 2 nanosecond (ns) are reported. Application abilities of commercial power rectifier diodes in the DSRD mode are shown. Transmitter based on DSRD can operate with low impedance antennas, high repetition rate and efficiency.

Key words: drift step recovery diode, ground penetration radar, nanosecond pulse generation.

INTRODUCTION

Ground penetrating radar (GPR) can be divided into some functional elements. There are transmitter, receiver, antennas set, control and computational unit and display. Transmitter is the most important component of the GPR and along with receiver and antennas it determines attainable performance factor, vertical resolution and depth of sounding.

Heart of the transmitter is subnanosecond pulse generator. As an active element of the scheme is usually utilized either avalanche diode (AD) or transistor (AT) or step-recovery diode (SRD). These devices are able to form subnanosecond pulses with high repetition rate and shape stability. However, their peak power range don't exceed one kilowatt level and these widely used active elements are not suitable for creation of high power GPR that is destined for operation in difficult environments. For sharpening of kilovolts pulses with rise times on the order of a few nanosecond are capable a new active elements - drift step recovery diodes (DSRDs).

The main goal of this work is theoretical consideration and experimental investigation of DSRD application possibilities as an active element of subnanosecond generator for high power GPR design.

PROPERTIES OF THE DRIFT STEP RECOVERY DIODES

Effect of high power nanosecond impulse generation by drift step-recovery diodes (DSRDs) has been discovered by Russian inventors in 1981 (Grekhov et al., 1981). In traditional SRD charge is stored in the diode by means of a nearly steady-state forward current flow. That is the forward bias exists continuously for times compared to or longer than the hole and electron lifetimes in the active region. Conversely high power DSRD uses a short forward bias pulse to introduce stored charge to the device. Since the pulse width is considerably less than the carrier lifetimes, the charge is concentrated near the junctions, which is desirable for a sharp reverse step recovery. These structures have been shown to be capable of operating at much higher power levels than conventional SRD structures. The DSRD have been found to be useful primarily above one kilovolts and offer lifetimes only somewhat better than conventional SRD. Brylevsky et al. (1988) thanks DSRD achieved peak powers more than 1.6 megawatt on 10-Ohm loading with two-nanosecond rise time.

The step-recovery effect in the DSRD can be observed only by satisfaction of specific conditions. Because charge carrier mobility in the drift diodes are low therefore current at the straight direction through the p-n junction not constant but briefly. Moreover straight time transition for the diodes with a long lifetime of the charge carriers has to be as short as possible. If diode has a short lifetime charge

carriers (approximately 500 nanosecond) current to the straight direction is only limited by p-n junction overheating and can be as long as 10 microsecond (Grekhov et al., 1984). There are a lot of commercial available diodes that can be used as DSRD (Zienko, 1984). Differences of the commercial high power diodes from ideal ones lead to efficiency decreasing and pulse shape distortion. These defects can be eliminated by carrying out the following conditions: a) forward current duration and brought into the p-n junction charge have to be as small as possible, and b) reverse current duration has to be considerably less (10 times and more) than forward current duration (Belkin et al., 1992).

Earlier DSRD (Zienko, 1984; Grekhov et al., 1986; Kardo-Sysoev and Chashnikov, 1986) are used as a sharpener of the step voltage generated by power semiconductor switchers (high power thyristor, for example). Thyristor is an optimal active element for step voltage generation if pulse duration is longer than its rise time. But thyristor is very low efficiency if pulse duration and rise time is comparable values. Losses of energy deal with thyristor switching losses and dissipation energy into the DSRD. Low efficiency and comparatively slow relaxation time peculiar to thyristors limit repetition rate of the device.

Therefore later Brylevsky et al. (1988) proposed to use intermediate inductance energy accumulator. Energy transmission from the inductance accumulator to loading has been realized by DSRD. In this case has been eliminated losses described earlier and increased efficiency of the generator. Peak voltage produced by generator was significantly exceeded power supply level. Using 50 Volts power supply has been achieved impulse voltage near 1300 Volt with 2-nanosecond rise time on the 50-Ohm loading. Efficiency of this scheme was more than 20 per cent, repetition rate up to 20 kHz.

Using of several switches complicate control circuits. Belkin et al. (1992) tried to simplify switching scheme. They used single switcher that transformed energy from power supply. Current reverse through DSRD has been provided with assistance of core saturated transformer. Using 100-150 Volt power supply they formed high voltage impulse (700-1000 Volts) with 1-1.5 nanosecond rise time on the 50-Ohm loading. Repetition rate was up to 50 kHz with efficiency up to 50 per sent.

It is clear the scheme decisions described above have been primarily made for experimental investigations of a step recovery effect in the high power diodes and can't be directly used for GPR application. Among of their common defects are complicated switching and control circuits, using of comparatively high voltage power supply.

MODELLING OF THE DRIFT STEP RECOVERY DIODES

Modeling of the power rectifier diodes is usually based on its static mode representation and doesn't take into account transient behavior during a switching process. There is also models based on physical characteristics of semiconductor materials and p-n junctions (M.J. Chudobiak, 1996). Although physical model sufficient precisely describes step recovery effect into drift diodes such one doesn't suitable for simulating of DSRD generator, based on commercially available elements. It is more preferable model that operates such integrated parameters, as current, voltage, capacitance and recovery time. Try to realize diode model assuming that its switching deals with charge into active region. Let's assume that the diode is described as:

$$u_d(t) = \begin{cases} r_d i_d(t), \ if \int_0^t i_d(\tau)d\tau \geq 0 \\ \frac{1}{C_d}\int_0^t i_d(\tau)d\tau, \ if \int_0^t i_d(\tau)d\tau < 0 \end{cases} \quad (1)$$

where
$i_d(t)$ - current through the diode,
$u_d(t)$ - voltage applied to the diode,
C_d - diode capacity under reverse bias voltage applied,
r_d - diode resistance under forward bias voltage applied.

It is a simplest model that doesn't take into account switching delay and nonlinearity of dependence $i_d(t)$ on $u_d(t)$ during forward biasing and breakdown effect at reverse one. However it this model is useful for analysis of the DSRDs control circuits.

Assume that DSRD is incorporated into the scheme (Figure1): E(t) - power supply voltage, provided forward and reverse current flow through the DSRD structure; L1 - isolated choke; C1 - separation capacitor; R1 - current limited resistor; R2 - loading resistor.

Principle of this circuit operation is following. At first some charge is pushed by short pulse of negative polarity into active region of the DSRD. Then voltage polarity is changed and primary charge is pulled out. At the moment when total charge will be equal zero diode quickly closed. Energy accumulated into the choke during action of pulse of positive polarity charge capacitors C_d and C1. Charged current appears on the loading resistor as output signal.

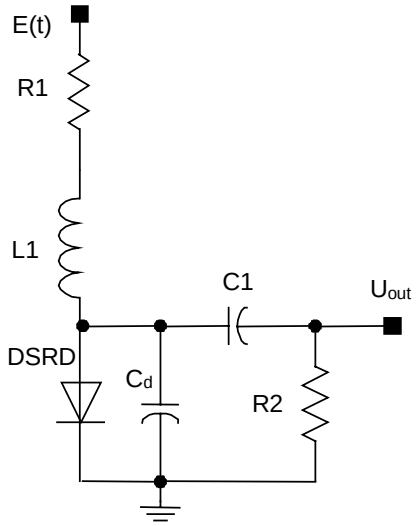

Figure 1: Driving circuit of the DSRD structure.

Let's write differential equation for this scheme:

$$E(t) = L_1 \frac{di(t)}{dt} + R_1 i(t) + u_d(t) \quad (2)$$

$$u_d(t) = R_2 i_l(t) + \frac{1}{C_1}\int_0^t i_l(\tau) d\tau \quad (3)$$

Taking in mind, that

$$i(t) = \frac{dQ(t)}{dt},\ i_d(t) = \frac{dQ_d}{dt},\ i_l(t) = \frac{dQ_l}{dt}, \quad (4)$$

$$i(t) = i_d(t) + i_l(t),\ Q(t) = Q_d(t) + Q_l(t)$$

Rewrite the equation (1) - (3) by using charges Q(t):

$$E(t) = L_1 \frac{d^2Q(t)}{dt^2} + R_1 \frac{dQ(t)}{dt} + u_d(t) \quad (5)$$

$$u_d(t) = R_2 \frac{dQ_l(t)}{dt} + \frac{Q_l(t)}{C_1} \quad (6)$$

$$u_d(t) = \begin{cases} r_d \dfrac{dQ_d(t)}{dt},\ if\ \ Q_d(t) \ge 0 \\ \dfrac{Q_d(t)}{C_d},\ if\ \ Q_d(t) < 0 \end{cases} \quad (7)$$

Replace Q(t) to $Q_l(t)$ and $Q_d(t)$ in the equation (5):

$$E(t) = \left(L_1 \frac{d^2}{dt^2} + R_1 \frac{d}{dt} \right)\left(Q_l(t) + Q_d(t)\right) + u_d(t) \quad (8)$$

Substituting $u_d(t)$ from (6) and (7) into (5) we get a system of the following equations:

$$\begin{cases} E(t) = U(t) + \left(R_2 \dfrac{d}{dt} + \dfrac{1}{C_1} \right) Q_l(t) \\ E(t) = U(t) + \begin{cases} r_d \dfrac{dQ_d(t)}{dt},\ if\ \ Q_d(t) \ge 0 \\ \dfrac{Q_d(t)}{C_d},\ if\ \ Q_d(t) < 0 \end{cases} \end{cases} \quad (9)$$

where

$$U(t) = \left(L_1 \frac{d^2}{dt^2} + R_1 \frac{d}{dt} \right)\left[Q_d(t) + Q_l(t)\right]$$

Use the finite-difference (FD) algorithm for solving these equations. Replaced derivatives to finite differences

$$\frac{dQ(t)}{dt} = \frac{Q_{n+1} - Q_{n-1}}{2\Delta t}, \quad (10)$$

$$\frac{d^2Q(t)}{dt^2} = \frac{Q_{n+1} - 2Q_{n1} + Q_{n-1}}{\Delta t^2}$$

and introduce the following abbreviations

$$\tau_1 = \frac{C_1 R_1}{2\Delta t},\ \tau_2 = \frac{C_1 R_2}{2\Delta t},\ \tau_d = \frac{C_1 r_d}{2\Delta t}, \quad (11)$$

$$w = \frac{C_1 L_1}{\Delta t^2},\ k_d = \frac{C_1}{C_d}$$

express (n+1)-th element of the charges $Q_{l_{n+1}}$ and $Q_{d\,n+1}$ in the circuit through the preceding ones in time domain. The resulted expressions for the charge behavior in the driving circuit are the following:

$$Q_{d_{n+1}} = \frac{\tau_2 \left[C_1 E_n + 2wQ_{d_n} + (\tau_1 - w)Q_{d_{n-1}} \right] + (\tau_1 + w)Q_{l_n} + if\,(Q_{d_n} \geq 0, \tau_d Q_{d_{n-1}}, -k_d Q_{d_n})}{\tau_2(\tau_1 + w) + if\,(Q_{d_n} \geq 0, \tau_d, 0)}$$

$$Q_{l_{n+1}} = \frac{C_1 E_n + (2w-1)Q_{l_n} + (\tau_1 + \tau_2 - w)Q_{l_{n-1}} - (\tau_1 + w)Q_{d_{n+1}} + 2wQ_{d_n} + (\tau_1 - w)Q_{d_{n-1}}}{\tau_1 + \tau_2 + w} \quad (12)$$

CALCULATION OF THE CHARGES BEHAVIOUR AT THE INVOLVED DSRD CIRCUIT

Using equations (4) - (6) we can easily take curves for voltages and currents in detail in any desirable point of the circuit knowing charges Q, Q_d and Q_l evolution.

Assume that a test voltage is bipolar step one based on high orders exponential function, that itself and its derivatives up to the third orders during numerical calculations have nowhere discontinuities and others indefinite points. Assume positive pulse duration is τ_+, and negative one is τ_-. Rise times for each of the pulses are equal τ.

Results of the diode transient simulation based on charge model are shown on Figure2. There are normalized driving voltage E, instantaneous charge Q, current through the diode i_d and voltage on the one u_d. These data are in a good agreement to real diodes behavior.

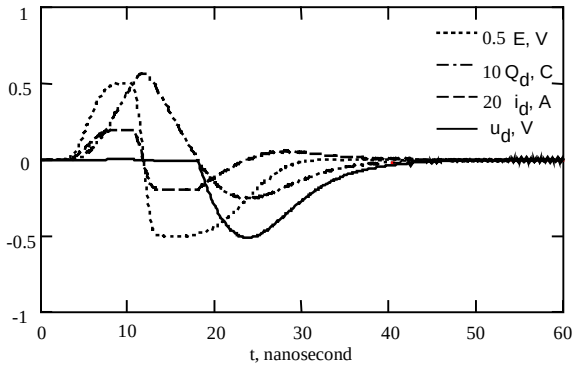

Figure 2. Charge and current behavior in the diode structure vs. excitation voltage.

Shape evolutions of the loading current with scheme parameters changing are presented on Figure 3. These curves show as impulse characteristics connected with changing of the driving circuit elements. Analysis of the data is allowed to make the following conclusions. The driving circuit works correctly if resistance R1 as against L1 is to be as low as possible. It is very important to take the diode with a minimal reverse voltage capacitance also. Volume of C1 capacitor depends from C_d but isn't to be too big because it causes to increasing of the pulse generation time delay. It is not any limits to the R2 loading resistor choice. Therefore this choice depends on environment requirements. As a result the DSRD can be used with both low impedance loading and high one.

EXPERIMENTAL RESULTS

Using described above driving circuit experimental testing of power rectifier diodes in the DSRD mode have been carried out. Series of 1N5408 impulse rectifier diodes (reverse voltage V_R=1000V, forward current I_F=3A, reverse recovery time t_{rr}=200 ns) was under investigation. Driving voltage parameters were the following: peak-to-peak voltage E=(E_++E_-)=100...400V, positive half-wave duration τ_+=300 ns, negative half-wave duration τ_-=200 ns, rise and fall time τ=60 ns, positive to negative voltage rate E_+/E_- =1/2.

During the series of the experiments have been got the following results. Minimum rise time was 1.6 nanosecond. As high maximum peak voltage as 550 Volts on the 50-Ohm loading has been achieved with applied 400-Volt peak-to-peak voltage. Driving impulse amplitude changing was not furnished with shape distortion. Power consumption was less than 6 Watts with 20 kHz pulse repetition rate. Repetition rate may be increased up to 100 kHz without generation characteristic deterioration by driver circuit modernization.

CONCLUSIONS

This work is mainly devoted to modeling of DSRD generator driving circuit and simulating of this process in the time-domain. The proposed model can be applied to study transient charge and currents behavior only. Analysis of the diode parameters and others scheme elements can be carried out also.

Simulation results are allowed to determine optimal parameters of the driver circuit taking into account parameters of the rectifier diode that has to be used in the DSRD mode.

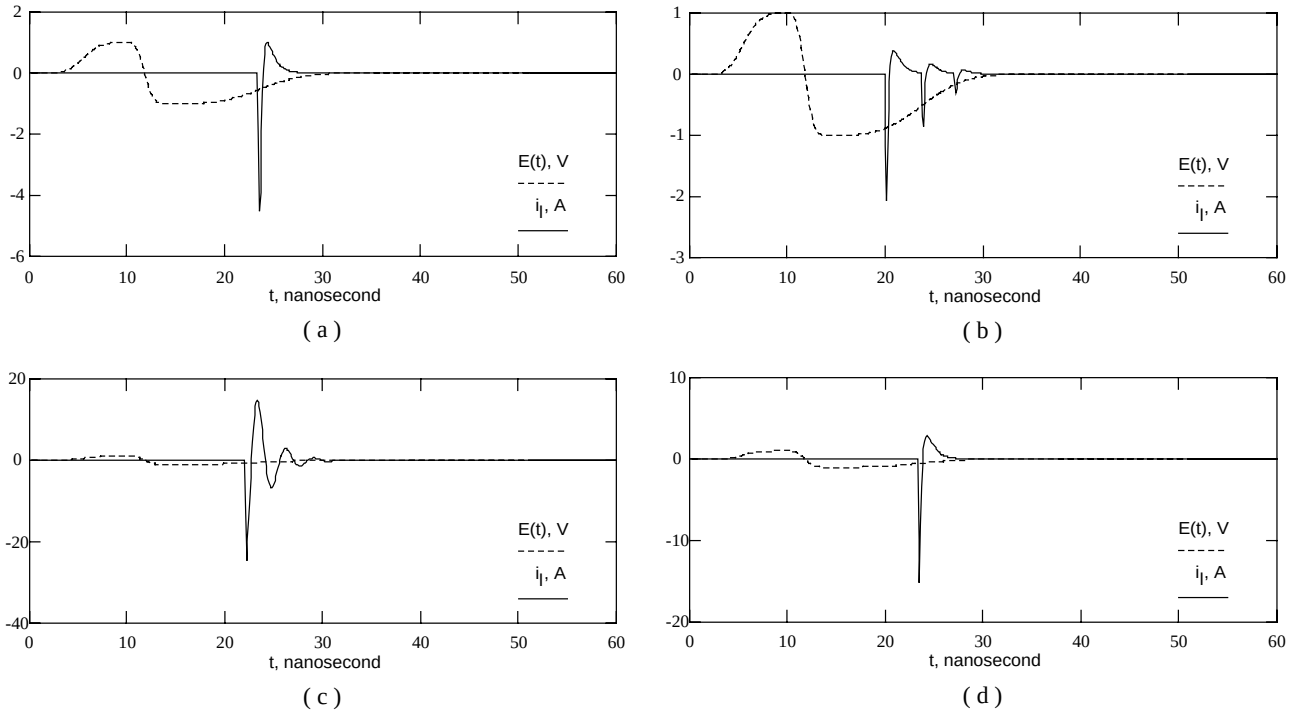

Figure 3. Evolution of the loading current i_l versus changing of the driving circuit parameters. a) loading current under initial conditions ($\tau1=0.1$; $\tau2=5$; $\tau_d=0,1$; $w=20$; $k_d=200$); b) multiply generation is observed by $\tau1$ or τd increasing or w decreasing; c) oscillations are observed by w increasing or $\tau2$ decreasing; d) peak power growth is happened by k_d increasing only.

Besides of experimental test of two type of the rectifier diode has been made too. Investigations have showed good correspondence calculations to the experimental results.

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